AF/2154 IFW

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Dated: August 2, 2004

Mark D. Saralino

Attorney Docket No. E0862 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:

Applicant:	Atul GARG, et al.	Art Unit:	2154
Serial No.:	09/644,464	Examiner:	Chad Zhong
Filed:	August 23, 2000		
Title:	NETWORK TRANSMITTER WITH DATA FRAME PRIORITY MANAGEMENT FOR DATA TRANSMISSION		

TRANSMITTAL OF APPEAL BRIEF

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Enclosed herewith is an Appeal Brief in triplicate, submitted with regard to the previously-filed appeal for the above application. A check for **$330.00** is enclosed for payment of the fee for submission of the Appeal Brief.

Authorization is given to charge any additional fees required in connection with any of these papers to our Deposit Account 18-0988.

Respectfully submitted,

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Docket No: E0862

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Atul GARG et al.
Serial No.:	09/644,464
Filing Date:	August 23, 2000
For:	NETWORK TRANSMITTER WITH DATA FRAME PRIORITY MANAGEMENT FOR DATA TRANSMISSION
Examiner:	Chad Zhong
Art Unit:	2154
Notice of Appeal:	July 12, 2004

APPEAL BRIEF

Mailstop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This brief is being submitted in connection with the appeal of the above-identified application.

I. Real Party in Interest

The real party in interest in the present appeal is Advanced Micro Devices, Inc., the assignee of the present application.

II. Related Appeals and Interferences

Appellant, appellant's legal representatives, and/or the assignee of the present patent are unaware of any appeals or interferences which will directly affect, or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. Status of Claims

Claims 1, 3-14 and 16-22 are pending in the application. Claims 1, 3-14 and 16-22 stand finally rejected and are the subject of this appeal.

IV. Status of Amendments

Claim amendments were made subsequent to the final rejection. The claim amendments were filed on April 21, 2004 in the response to the final Office Action, and the claim amendments were entered by the Examiner for purposes of this Appeal.

V. Summary of Invention Defined in the Claims on Appeal

The present invention relates to a frame processing unit for prioritizing data frames for transmission on a network medium. With reference to Fig. 3 of the present application (reproduced below), frame processing unit 74 receives real time data frames and non-real time data frames from peripheral bus 44. Frame processing unit 74 includes a frame buffer management circuit 100 to manage data frames, a random access memory frame buffer 102 for storing incoming data frames, and a priority and address random access memory pointer table 104 to reference data frames. Frame processing unit 74 also includes a register 106 for storing an indicator representing the priority of frames available for transmission, a priority resolution circuit 108 for selecting the highest priority data frame available for transmission (or the priority data frame requested by the media access controller), and a frame transmission circuit 110 for retrieving data frames from the frame buffer 102 and transmitting data frames to a media access controller 72.[1]

In operation, the frame buffer management circuit 100 reads incoming data frames received from peripheral bus 44 and writes the data frames to the random access memory frame buffer 102. Further, the frame buffer management circuit 100 writes, to the pointer table 104, the start address and end address corresponding to

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1. Page 9, lines 6-16 of the present application

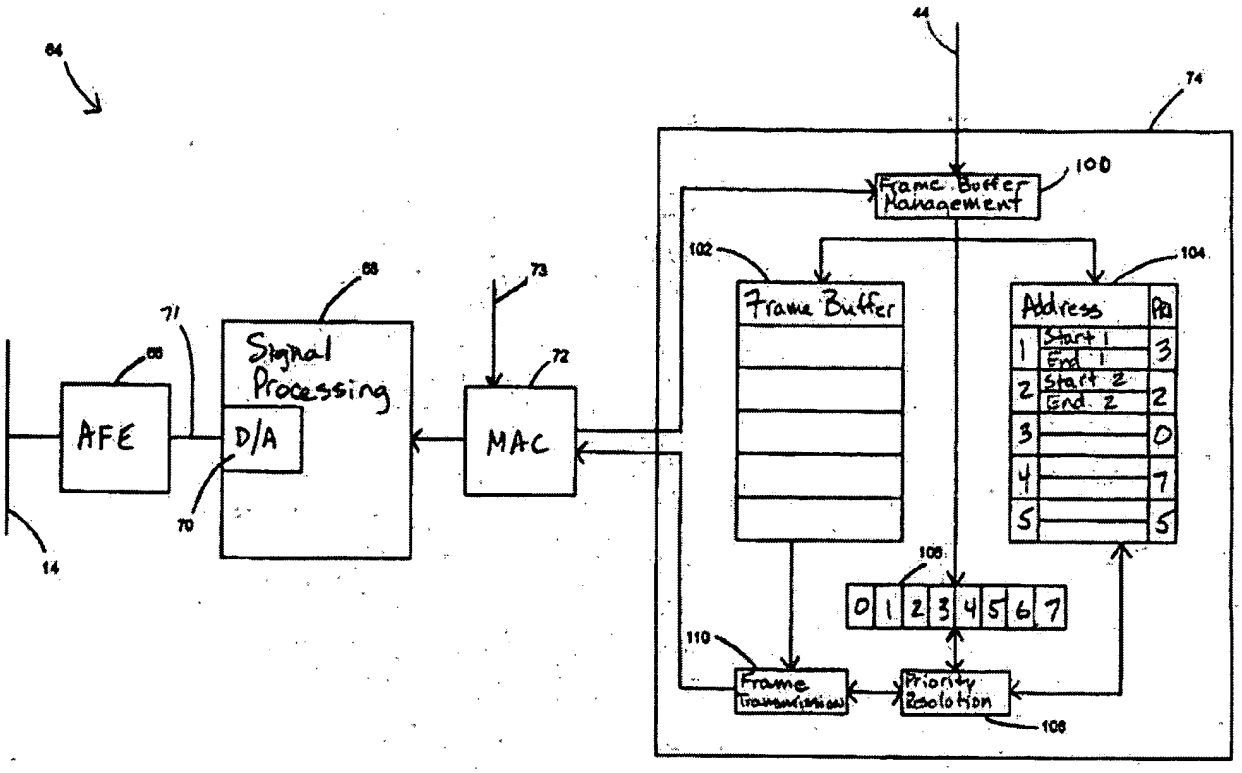

Figure 3

where the data frame was stored in the frame buffer 102 along with the corresponding priority level. The frame buffer management circuit 100 also sets a bit in the register 106 corresponding to the priority level.[2]

The priority resolution circuit 108 reads the register 106 to determine the highest priority data frame available for transmission, retrieves the frame's address from the random access memory pointer table 104, and sends the data frame's address to the frame transmission circuit 110.[3]

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2. Page 9, lines 17-23 of the present application

3. Page 9, lines 24-27 of the present application

The media access controller 72 receives a signal from channel sensor circuitry (not shown) on line 73 indicating that the network medium 14 is available for transmission. Upon receipt of such signal, the media access controller 72 generates a data frame request to the frame transmission circuit 110.[4]

The frame transmission circuit 110, upon receiving the data frame request signal from the media access controller 72, retrieves the data frame from the random access memory frame buffer 102 (which has been updated by the priority resolution circuit 108) and presents the data frame to the media access controller 72.[5] Upon transmitting the data frame, the frame transmission circuit 110 issues a signal to the priority resolution circuit 108. The priority resolution circuit 108, upon receiving the signal, clears the register 106, the random access memory frame buffer 102 and the random access memory pointer table 104.[6]

If the priority resolution circuit 108 does not receive the signal from the frame transmission circuit 110, the priority resolution circuit 108 rereads the register 106 to determine whether a higher priority data frame (or a frame with the priority requested by the media access controller) is available. If there is no such frame, then the priority resolution circuit 108 again waits for the signal from the frame transmission circuit 110 to clear the register 106. If there is such a data frame available, the priority resolution circuit 108 retrieves the address of such data frame from the random access memory pointer table 104, and the priority resolution circuit 108 writes the data frame's address to the frame transmission circuit 110.[7]

Accordingly, the present invention operates to assure that any address written to the frame transmission circuit 110 can be overwritten with an address of a higher priority frame at any time prior to actual transmission to the MAC and the priority

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4. Page 10, lines 14-17 of the present application

5. Page 9, line 30 through page 10, line 2 of the present application

6. Page 12, lines 16-20 of the present application

7. Page 11, line 23 through page 12, line 3 of the present application

resolution circuit receiving the clear signal. In other words, a data frame that has been designated for transmission can be replaced, prior to transmission, with a new data frame having a higher priority.

VI. Issues

A. Whether claims 1, 3-14 and 16-22 are patentable under 35 U.S.C. §102(b) over U.S. Patent No. 5,043,981 to *Firoozmand et al.* (hereinafter *Firoozmand*).

B. Whether claims 1, 3-14 and 16-22 satisfy the requirements of 35 U.S.C. §112, second paragraph.

VII. Grouping of Claims

For the purposes of this appeal only, the claims are grouped as follows:[8]

i. Claims 1, 3-14 and 16-22 stand or fall together.

VIII. Argument

1. Rejection of claims 1,3-14 and 16-22 under 35 USC §102(b)

Claims 1, 3-14 and 16-22 stand rejected under 35 USC §102(b) based on *Firoozmand.* For the following reasons, it is respectfully submitted that the claims are patentable over the applied art and the final rejection should be withdrawn.

a. Claims 1, 3-6, 10-12, 14 and 16-19

Claims 1, 3-6, 10-12, 14 and 16-19 stand rejected under 35 USC §102(b) based on *Firoozmand.* Reversal of the rejection is respectfully requested for at least the following reasons.

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8. This grouping is conditioned upon the Examiner not entering any new grounds of rejection and/or any new points of argument.

Claims 1 and 14 recite the feature of the invention whereby the priority resolution circuit continually retrieves data from the register to determine a highest priority data frame in the buffer memory and *replaces the address previously provided to the frame transmission circuit if a higher priority frame becomes available*. Similarly, claim 10 recites a method which includes *overwriting the address of the highest priority data frame with an address of a new highest priority data frame if a new higher yet priority data frame becomes available*.

As is discussed in the background section of the present application, it is known to prioritize data frames within a queue.

> However, prioritizing frames within a queue does not resolve a front of line blocking problem. A front of line blocking problem occurs when, for example, the highest priority data frame (say priority 3) is retrieved from a queue and is written to a register (or other memory) for transmission in the next available time slot (e.g. interval of time available to the media access controller for transmission). At this time, that data frame is isolated from the remaining data frames left in the queue. The remaining data frames in the queue may be reprioritized with newer, incoming data frames, however, no other frames can be transmitted until that first data frame is transmitted. Hence, a higher priority data frame (say 6) which has come into the queue after the first frame was written to the register is blocked from transmitting before the lower priority data frame 3. [9]

The present invention as recited in claims 1, 10 and 14 overcomes such problem associated with front of line blocking by virtue of a priority resolution circuit continually retrieving data from the register to determine a highest priority data frame in the buffer memory and replacing the address previously provided to the frame transmission circuit if a higher priority frame becomes available.

The Examiner contends that *Firoozmand* teaches such feature. The Examiner contends that *Firoozmand* teaches a priority resolution circuit which continually retrieves data from the register to determine the highest priority data frame in the buffer

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9. Page 2, lines 17-27 of the present application

memory. More specifically, the Examiner contends that *Firoozmand* teaches that the priority resolution circuit continually retrieves the data *and replaces the address previously provided to the frame transmission circuit if a higher priority frame becomes available*. Applicants respectfully disagree, and will address each of the Examiner's points below.

i.

Firoozmand does not teach or suggest a system or method which involves a priority resolution circuit continually retrieving data from a register to determine a highest priority data frame in the buffer memory and replacing the address previously provided to the frame transmission circuit if a higher priority frame becomes available as recited in claims 1, 10 and 14. *Firoozmand* does not address the front of line blocking problem with which the present invention is concerned.

Rather, *Firoozmand et al.* is concerned with a different kind of problem relating to "lock up". Specifically, the FIFO memory "locks up" when the amount of storage remaining available in the logical FIFO containing the queue is less than the storage capacity of the physical FIFO.[10] *Firoozmand et al.* describes a network DMA controller 124 designed to monitor the FIFO queue. If a queue becomes full, the packet buffer management circuit 156 locks the queue to finish emptying the current FIFO and to suspend the queue. If a transfer is incomplete, the circuit 156 continues with other pending transfers until receiving a signal that the queue becomes unlocked.

The Examiner notes that synchronous data in *Firoozmand* have higher priority over asynchronous data. The Examiner further notes that it is well known in the art that different data packets with varying priorities arrive at random times at the buffers. Applicants agree with the Examiner in this regard.

The Examiner goes on to state that ergo, continuous monitoring and retrieval of data packets based on priorities for transmission from the buffers is realized. To the

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10. Column 2, lines 17-23 of Firoozmand

extent that the Examiner is stating that it is well known in the art to continue to sense and provide higher priority data packets to the transmission circuit ahead of lower priority data packets, applicants again agree with the Examiner.

However, claims 1, 10 and 14 refer to continually retrieving data from the register to determine a highest priority data frame in the buffer memory and *replacing the address previously provided to the frame transmission circuit if a higher priority frame becomes available*. The present invention is addressing the front of line blocking which occurs when the frame transmission circuit is provided with the address of the highest priority data frame and then, *prior* to the frame transmission circuit actually transmitting the highest priority data frame, an even higher priority data frame is placed in the buffer memory.

According to the present invention, the address of the highest priority data frame provided to the frame transmission circuit is *replaced* with the address of the data frame now having an even higher priority. This way, when the frame transmission circuit is eventually granted access to the system bus, etc., the data frame having the even higher priority will be transmitted *before* the original highest priority data frame.

In *Firoozmand* as well as the other conventional art referred to by the Examiner, the address of the highest priority data frame provided to the frame transmission circuit is not *replaced* with the address of the data frame now having an even higher priority. Rather, the frame transmission circuit retains the address of the highest priority data frame until the frame transmission circuit acquires access to the system bus and the highest priority data frame is transmitted. *Then*, the frame transmission circuit is subsequently provided with the address of the data frame having the even higher priority. The frame transmission circuit then transmits the data frame having the even higher priority.

Thus, in *Firoozmand* the original highest priority data frame will be transmitted prior to the data frame having the even higher priority. This front of line blocking situation is exactly opposite of the claimed invention. This is because the address provided to the frame transmission circuit in *Firoozmand* is not being *replaced* in the

event an even higher priority data frame is found in the buffer memory. Rather, the address of the even higher priority data frame is simply the next, or subsequent, address provided to the frame transmission circuit.

It will therefore be appreciated that Column 13, lines 13-17 of *Firoozmand*, which was cited by the Examiner as teaching the claimed invention, simply relates to the priority at which packets are transmitted. Specifically, *Firoozmand* describes how, when the transmitting device receives the token, the transmitting device transmits the synchronous data first. This is because the synchronous data has higher priority than non-synchronous data. Such transmission of the synchronous data before non-synchronous data based on priority is very conventional and not the focus of the invention. There is no replacing of the address provided to the frame transmission circuit as discussed above.

According to *Firoozmand*, for example, if the synchronous queue (highest priority) were empty (e.g., all data had been transmitted) and each asynchronous queue had data, the device would serially move each data frame from an asynchronous queue having the highest priority to the frame transmission circuit and, upon receiving the token, the frame transmission circuit would transmit each respective data frame. Upon emptying the highest priority asynchronous queue, the device now would move to the asynchronous queue having the next highest priority. Again, each data frame would be serially moved into the frame transmission circuit and subsequently transmitted upon receiving the token.[11]

If synchronous data should arrive in the synchronous queue while asynchronous data were in the frame transmission circuit, the synchronous data would not be transferred on the next rotation of the token, since the frame transmission circuit of *Firoozmand* must first transmit the data therein prior to accepting the new "higher priority" synchronous data. Instead, the high priority synchronous data is delayed one token rotation time before being transmitted. Once data is slated for transmission, it

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11. Column 13, lines 13-25 of Firoozmand

cannot be retrieved. Thus, the device of *Firoozmand* exhibits a front of line blocking problem that the present invention addresses.

ii.

Regarding Column 8, lines 10-40[12], the Examiner notes that "when a new data packet coming in from synchronous queue as is done in *Firoozmand* it gets a higher priority and 'jump' ahead of the remainder of the packets are currently present (if any), and gets processed".[13]

Again, applicants agree with the Examiner that new data packets from the synchronous queue in *Firoozmand* have higher priority and "jump" ahead of the remainder of the packets which are currently present. This is the same general priority scheme that is well known in the art as pointed out by the Examiner and discussed above.

Column 8, lines 10-40 of *Firoozmand* discusses operation of the transmit section 152 in the DMA controller 124. The transmit section 152 transfers data stored therein to the output buffer memory 126 via an interface 150.[14] A packet buffer management circuit 156 indicates to the medium access controller 120 what type of data is present in the transmit section, so as to load the buffer memory 126 in appropriate queues depending on the priority in accordance with the FIFO specifications.

The packet buffer management circuit 156 prioritizes command requests, transmit requests from the FIFO 152 and receive requests from the FIFO 154. The management circuit then issues commands to a system memory interface 160 to grant either transmits or receives or to process one of the commands. Transmit section FIFO 152 maintains all transmit queues and prioritizes operations in a predetermined priority.

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12. Cited by the Examiner in the final Office Action dated April 14, 2004, page 4, line 13

13. Page 7, lines 19-21 of Office Action dated April 14, 2004

14. Column 7, lines 46-64; Fig. 8 of Firoozmand

The transmit section FIFO 152 carries out byte ordering and data gathering, and formats the data into FIFO oriented packets to be processed by the medium access controller 120.

With respect to packets transmitted from the transmit section FIFO 152 to the buffer memory 126, *Firoozmand* teaches that the packet buffer management circuit 156 prioritizes the requests. The transmit section FIFO 152 maintains all transmit queues and prioritizes operations in a predetermined priority.[15]

The Examiner has not shown where in *Firoozmand* it is taught or suggested that the transmit section FIFO 152 or the packet buffer management circuit 156 include any type of priority resolution circuit that continually retrieves data from the register to determine a highest priority data frame in the buffer memory and *replaces* the address previously provided to the frame transmission circuit *if a higher priority frame becomes available*.

Frankly, *Firoozmand* has not been shown to even describe the priority resolution operation therein in sufficient detail that it could even be suggested that *Firoozmand* teaches the claimed invention. Again, prioritization between data frames (e.g., synchronous vs. asynchronous) is not new and nor is it considered the invention. Rather, the invention relates to the manner in which a data frame, previously slated for transmission by virtue of its address being provided to a priority resolution circuit so that the data frame is made available to the media access controller for transmitting, is not transmitted by virtue of its address being *replaced* by an address of a higher priority frame as discussed above. There simply is no such teaching or suggestion in *Firoozmand.*

iii.

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15. Column 8, lines 1-40 of Firoozmand

Regarding "locking up" in *Firoozmand* , the Examiner submits that the prevention of "locking up" in *Firoozmand* is related to the front of line blocking problem which the applicants are trying to solve.[16] Applicants respectfully disagree in this regard.

Firoozmand is concerned with "lock up" as pointed out by the Examiner. However, such "lock up" does not involve the front of line problem addressed by the present invention. More importantly, such "lock up" does not in any way involve continually retrieving data from a register to determine a highest priority data frame in the buffer memory and replacing the address previously provided to a frame transmission circuit if a higher priority frame becomes available, as recited in claims 1, 10 and 14.

Specifically, *Firoozmand* describes how the FIFO memory "locks up" when the amount of storage remaining available in the logical FIFO containing the queue, is less than the storage capacity of the physical FIFO.[17] *Firoozmand* describes the network DMA controller 124 as designed to monitor the FIFO queue. If the queue becomes full, the packet buffer management circuit 156 locks the queue to finish emptying the current FIFO and to suspend the queue. If a transfer is incomplete, the circuit 156 continues with other pending transfers until receiving a signal that the queue becomes unlocked. Such "locking" and "flushing out" of the queue in no way relates to the presently claimed invention whereby an address provided by the priority resolution circuit is replaced with another address if a higher priority frame becomes available.

Again, the present invention is not concerned with basic prioritization as repeatedly referred to by the Examiner. Rather, the present invention addresses the front of line blocking problem associated with basic prioritization. The present invention avoids such problem by virtue of a unique configuration whereby the priority resolution circuit continually retrieves data from the register to determine a highest priority data

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16. Page 7, lines 22-25 of Office Action dated April 14, 2004

17. Column 2, lines 17-23 of Firoozmand

frame in the buffer memory and *replaces* the address previously provided to the frame transmission circuit if a higher priority frame becomes available.

Accordingly, reversal of the rejection of claims 1, 10, 14 and the claims dependent therefrom is respectfully requested.

2. Rejection of claims 1,3-14 and 16-22 under 35 USC §112, second paragraph

Claims 1, 3-14 and 16-22 stand rejected under 35 USC §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Specifically, the Examiner notes that the claims are indefinite with respect to points a (i thru iii) as set forth on pages 2-3 of the Office Action dated April 14, 2004.

The Applicant respectfully submits that amendments were made to claims 1, 7, 11, 14 and 20 to address each of the Examiner's concerns in point a (i). Claim 23 has been canceled and thus the rejection with respect to point a (iii) is moot. The amendments and cancellation were made in the reply to the final Office Action dated April 14, 2004, and the Examiner entered the amendments.[18]

As for point a (ii), claim 14, line 3 does not appear to include the phrase "an address". Applicants are uncertain exactly what changes the Examiner feels are appropriate. The Applicant's requested that the Examiner provide clarification regarding this point.[19] Clarification, however, was not provided in the Advisory Action.

Additionally, the Examiner did not indicate whether the amendments filed in the Reply to the Office Action removed the rejection under 35 U.S.C. §112, second paragraph.

Applicant believes that the pending claims meet the requirements of 35 U.S.C. §112, second paragraph. Furthermore, in the Advisory Action, the Examiner did not indicate that the rejection under 35 U.S.C. §112, second paragraph was maintained.

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18. See Reply to Office Action dated April 14, 2004, pages 6 and Advisory Action dated May 5, 2004, item 7.

19. See Reply to Office Action dated April 14, 2004, page 7, 4th paragraph

Accordingly, reversal of the rejection of claims 1, 3-14 and 16-22 is respectfully requested.

Conclusion

In view of the foregoing, appellant respectfully submits that the claims are patentable over the applied art and that the final rejection should be reversed.

Respectfully submitted,

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CERTIFICATE OF MAILING

I hereby certify that this paper (along with any paper or item referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as first-class mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

Date: August 2, 2004

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APPENDIX
CLAIMS ON APPEAL

1. A frame processing unit for transmitting data frames of varying priorities on a network medium comprising:

a) a frame buffer management circuit receiving data frames and storing data frames in a buffer memory;

b) a register storing data representing the existence of data frames of a designated priority in the buffer memory;

c) a priority resolution circuit, reading the register to determine a highest priority data frame available for transmission; and

d) a frame transmission circuit receiving an address of the highest priority data frame from the priority resolution circuit, receiving a signal from a media access controller indicating that the data frame may be transmitted, retrieving the data frame from the buffer memory corresponding to the address, and making the data frame available to the media access controller for transmitting to the network medium,

wherein the priority resolution circuit continually retrieves data from the register to determine a highest priority data frame in the buffer memory and replaces the address previously provided to the frame transmission circuit if a higher priority frame becomes available.

3. The frame processing unit of claim 1, wherein the frame buffer is a random access memory frame buffer.

4. The frame processing unit of claim 3, further including a random access memory pointer table storing an indicator of the priority for each frame in the frame buffer along with an address location of each frame in the frame buffer.

5. The frame processing unit of claim 4, wherein the frame buffer management circuit locates the address of the highest priority frame, as indicated by the register, from the random access memory pointer table.

6. The frame processing unit of claim 5, wherein the media access controller receives the frame from the frame transmission circuit and makes each frame available to physical layer circuitry.

7. The frame processing unit of claim 6, wherein the frame transmission frame circuit, upon transmission of the data frame to the media access controller, sends a command to the priority resolution circuit which in turn updates the register and the random access memory pointer table to reflect transmission of the data frame.

8. The frame processing unit of claim 7, wherein the frame buffer management circuit receives and stores data frames from an application via a peripheral bus.

9. The frame processing unit of claim 8, wherein data received via the peripheral bus may include data of varying priorities as assigned by the application.

10. A method of transmitting a highest priority data frame available for transmission in a frame buffer, the method comprising:

a) reading data from a register to determine a priority of the highest priority data frame available for transmission;

b) locating an address at which the highest priority frame is stored in a frame buffer;

c) writing the address of the highest priority data frame to a frame transmission circuit;

d) overwriting the address of the highest priority data frame with an address of a new highest priority data frame if a new higher yet priority data frame becomes available; and

e) retrieving the new highest priority data frame from the frame buffer and transmitting the new highest priority data frame when the network media is available.

11. The method of claim 10, further including updating the register upon transmission of the data frame to reflect transmission of the data frame.

12. The method of claim 11, wherein the step of locating the frame buffer address includes looking up the frame buffer address in a pointer table which stores the frame buffer address along with the priority of the frame stored at the address.

13. The method of claim 12, further including updating the pointer table upon transmission of a data frame to reflect transmission of the data frame.

14. A network computer comprising:

a) a central processing unit operating a plurality of applications generating data frames of varying priorities for transmission on a network medium;

b) a network interface circuit receiving the data frames and transmitting the data frames on the network medium in priority order, the network interface circuit including:

i) a frame buffer management circuit receiving data frames from the central processing unit and storing data frames in a buffer memory;

ii) a register storing data representing the existence of data frames of a designated priority in the buffer memory;

iii) a priority resolution circuit, reading the register to determine a highest priority data frame available for transmission; and

iii) a frame transmission circuit receiving an address of the highest priority data frame from the priority resolution circuit, receiving a signal from a media access controller indicating that the data frame may be transmitted, retrieving the data frame from the buffer memory corresponding to the address, and making the data frame available to the media access controller for transmitting to the network medium,

wherein the priority resolution circuit continually retrieves data from the register to determine highest priority data frame in the buffer memory and replaces an address previously provided to the frame transmission circuit if a higher priority frame becomes available.

16. The network computer of claim 14, wherein the frame buffer is a random access memory frame buffer.

17. The network computer of claim 16, further including a pointer table storing an indicator of the priority for each frame in the frame buffer along with an address location of each frame in the fame buffer.

18. The network computer of claim 17, wherein the frame buffer management circuit locates the address of the highest priority frame, as indicated by the register, from the random access memory pointer table.

19. The network computer of claim 18, wherein the media access controller receives the frame from the frame transmission circuit and makes each frame available to physical layer circuitry.

20. The network computer of claim 19, wherein the frame transmission circuit, upon transmission of the data frame to the media access controller, sends a command to the

priority resolution circuit which in turn updates the register and the random access memory pointer table to reflect transmission of the data frame.

21. The network computer of claim 20, wherein the frame buffer management circuit receives and stores data frames from an application via a peripheral bus.

22. The network computer of claim 21, wherein data received via the peripheral bus may include data of varying priorities as assigned by the application.